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TM8797

Demo Board Ver2.1

Specification

User Manual

Rev 2.3

AMENDMENT HISTORY

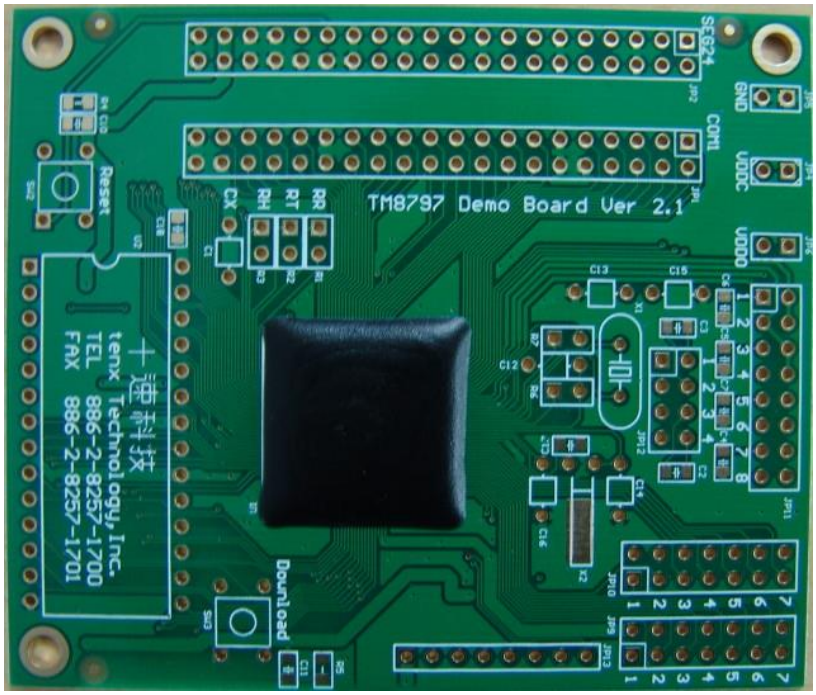
Version	Date	Description
V2.3	2008/07	1. 修改 Demo Board “Ver2.2” 為 “Ver2.1”(第二頁等)。 2. 修改產品示意圖於第 2 頁。 3. 修改 Doc No.原為”UM-TM8797_E”,改為: ”UM-TM8797DemoBoardV2.1_E” 。

CONTENTS

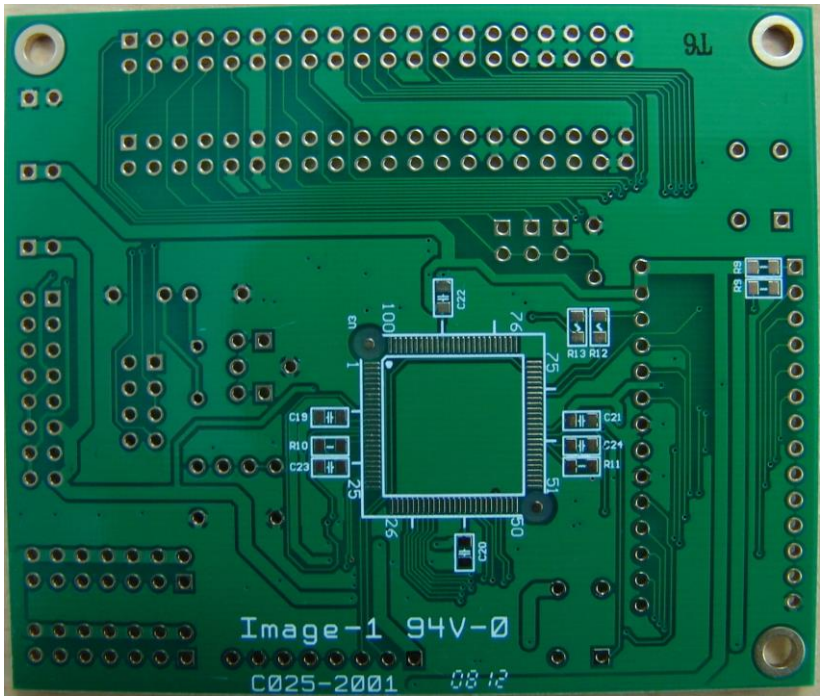
1. TM8797 DEMO board Ver 2.1 could support following chips directly: TM8720, TM8721, TM8722, TM8723, TM8724, TM8725, TM8726, TM87P04, TM87P08, TN87R04, TM87R08

2. TTM8797 Demo Board Ver 2.1 Figures:

2-1. TOP View:



2-2. Bottom View:



3. Parts Location & Description:

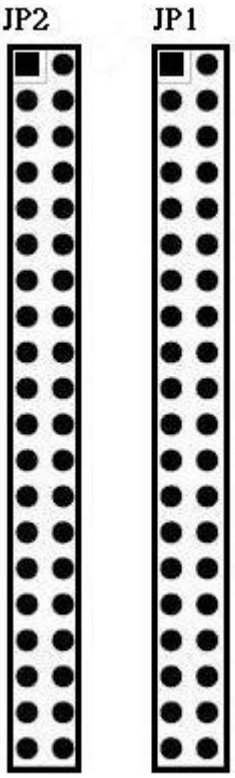
Item	Parts ref.	Description	Parts type
1	U1	TM8797 EV chip	COB
2	U2	Program ROM: For 27C256/28C256, starting address is 4000H For 27C512/28C512, starting address is C000H	28pin DIP
3	SW2	Reset key	Push button
4	R4	RC for Reset key	0805
5	C10	RC for Reset key	0805
6	SW3	Download key	Push button
7	R5	RC for Download key	0805
8	C11	RC for Download key	0805
9	JP1	COM1~9 & SEG1~23 I/O connector	40pin IDC
10	JP2	SEG24~41 & Reset & INT & VDDO connector	40pin IDC
11	JP4	External 5V input for EV chip & ROM interface	2pin Jumper
12	JP5	Power ground	2pin Jumper
13	JP6	Working voltage input for EV chip	2pin Jumper
14	JP9	Mask option sw1~sw7	14pin Jumper
15	JP10	Mask option sw8~sw14	14pin Jumper
16	JP11	Vdd1~4 CAP selection	16pin Jumper
18	C4~C7	CAP for Vdd1~4	104 / 0805
19	JP12	CUP0~2 CAP selection	8 pin Jumper
20	C2	For CAP0,CAP1	104 / 0805
21	C3	For CAP1,CAP2	104 / 0805
22	X2	Slow clock used crystal (32.768kHz)	Crystal
23	C14	EV chip XOUT CAP	
24	C16	EV chip XIN CAP	
25	R6	Slow clock used external RC	
26	C12	Slow clock used external RC	
27	X1	Fast clock used crystal or resonator (3.58MHz)	Resonator
28	C13	EV chip CFOUT CAP	
29	C15	EV chip CFIN CAP	
30	R7	Fast clock used external RC	
31	C17	BAK CAP connect to GND	104 / 0805
32	R1	RR connect to RFC circuit	
33	R2	RT connect to RFC circuit	
34	R3	RH connect to RFC circuit	
35	C1	CX connect to RFC circuit	

☆☆ Program ROM:
For 27C256/28C256, starting address is 4000H
For 27C512/28C512, starting address is C000H

4. I/O connector JP1 & JP2 Pin Description:

JP2	
SEG24	SEG25
SEG26	SEG27
GND	GND
SEG28	SEG29
SEG30	SEG31
GND	GND
SEG32	SEG33
SEG34	SEG35
GND	GND
SEG36	SEG37
SEG38	SEG39
GND	GND
SEG40	SEG41
GND	GND
RESET	GND
INT	GND
GND	GND
GND	GND
VDDO	VDDO
GND	GND

JP1	
COM1	COM2
COM3	COM4
COM5	COM6
COM7	COM8
COM9	GND
GND	GND
SEG1	SEG2
SEG3	SEG4
SEG5	SEG6
SEG7	SEG8
SEG9	SEG10
SEG11	SEG12
SEG13	SEG14
SEG15	SEG16
GND	GND
SEG17	SEG18
SEG19	SEG20
SEG21	SEG22
SEG23	GND
GND	GND

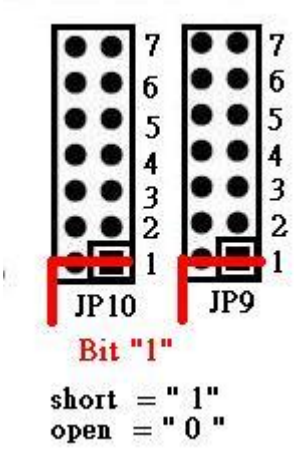


5. The selection bits of Mask option:

Some of the mask options are defined on JP10 and JP9.
When the left side hole and right side hole are shorted in each bit on JP10 or JP9, the bit will be set to 1.
If the holes are opened in each bit on JP10 or JP9, the bit will be set to 0.

Bit7
Bit6
Bit5
Bit4
Bit3
Bit2
Bit1
JP10

Bit7
Bit6
Bit5
Bit4
Bit3
Bit2
Bit1
JP9

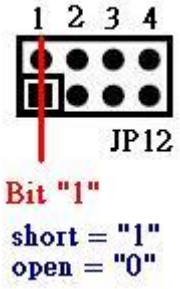


The following table showns the definition of each bit on JP10 and JP9:

Bit		JP10 bit definition	Bit		JP9 bit definition
1	**2**	Option for PH0<->BCLK in FAST ONLY MODE	**1**	**2**	Option for POWER SOURCE
0	0	PH0=BCLK	0	0	EXT-V
0	1	PH0=BCLK/4	0	1	3V BATTERY OR HIGNER
1	0	PH0=BCLK/8	1	X	1.5V BATTERY
1	1	PH0=BCLK/16			
3		Option for POWER ON RESET	**3**	**4**	Option for FAST/SLOW
			0	0	FAST ONLY
0		USE	0	1	SLOW ONLY
1		NO USE	1	X	DUAL
4	**5**	Option for LCD/LED ACTIVE MODE	**5**		Option for SLOW Clock Source
0	0	LCD	0		32.768KHz X'tal
0	1	LED HIGH ACTIVE			
1	0	LED LOW ACTIVE	1		RC
1	1	O/P			
6	**7**	Option for BIAS	**6**	**7**	Option for Fast Clock Source
0	0	No Bias	0	0	Internal R (250KHz)
0	1	1/2Bias	0	1	Internal R (500KHz)
1	0	1/3Bias	1	0	External R
1	1	1/4Bias	1	1	3.58MHz ceramic resonator

6. JP12 Setting for the capacitor connection of CUP0, CUP1 and CUP2:

This setting will define the LCD bias for the application.



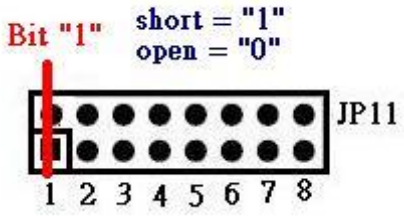
When the upper side hole and lower side hole are shorted in each bit on JP12, the bit will be set to 1.
If the holes are opened in each bit on JP12, the bit will be set to 0.

The following table shows the definition of each bit on JP12:

JP12 setting for the capacitor connection of CUP0,1,2				
Setting	**Bit1**	**Bit2**	**Bit3**	**Bit4**
DC	0	0	0	0
1/2 BIAS	1	1	0	0
1/3 BIAS	1	1	0	0
1/4 BIAS	1	1	1	1
	C3		C2	

When both bit1 and bit2 are set to 0 means C3 is unused.
When both bit1 and bit2 are set to 1 means C3 is connected to CUP0 and CUP1.
When both bit3 and bit4 are set to 0 means C2 is unused.
When both bit3 and bit4 are set to 1 means C2 is connected to CUP1 and CUP2.

7. JP11 Setting for the capacitors connection on VDD1,VDD2,VDD3,VDD4:



When the upper side hole and lower side hole are shorted in each bit on JP11, the bit will be set to 1.
If the holes are opened in each bit on JP11, the bit will be set to 0.

The following table shows the definition of each bit on JP11:

JP11 setting for the capacitors connection on VDD1,VDD2,VDD3,VDD4								
Setting	**Bit1**	**Bit2**	**Bit3**	**Bit4**	**Bit5**	**Bit6**	**Bit7**	**bit8**
AG 1/2	0	1	0	1	1	0	0	1
AG 1/3	0	1	1	0	1	0	0	1
AG 1/4	1	0	1	0	1	0	0	1
LI 1/2	0	1	0	1	0	1	1	0
LI 1/3	0	1	1	0	0	1	1	0
LI 1/4	1	0	1	0	0	1	1	0
DC	0	1	0	1	0	1	0	1

AG 1/2 : 1.5V power mode with 1/2 bias for LCD driver.
AG 1/3 : 1.5V power mode with 1/3 bias for LCD driver.
AG 1/4 : 1.5V power mode with 1/4 bias for LCD driver.

LI 1/2 : 3.0V power mode with 1/2 bias for LCD driver.
LI 1/3 : 3.0V power mode with 1/3 bias for LCD driver.
LI 1/4 : 3.0V power mode with 1/4 bias for LCD driver.

DC : 1.5V or 3.0V power mode without bias for LCD driver.